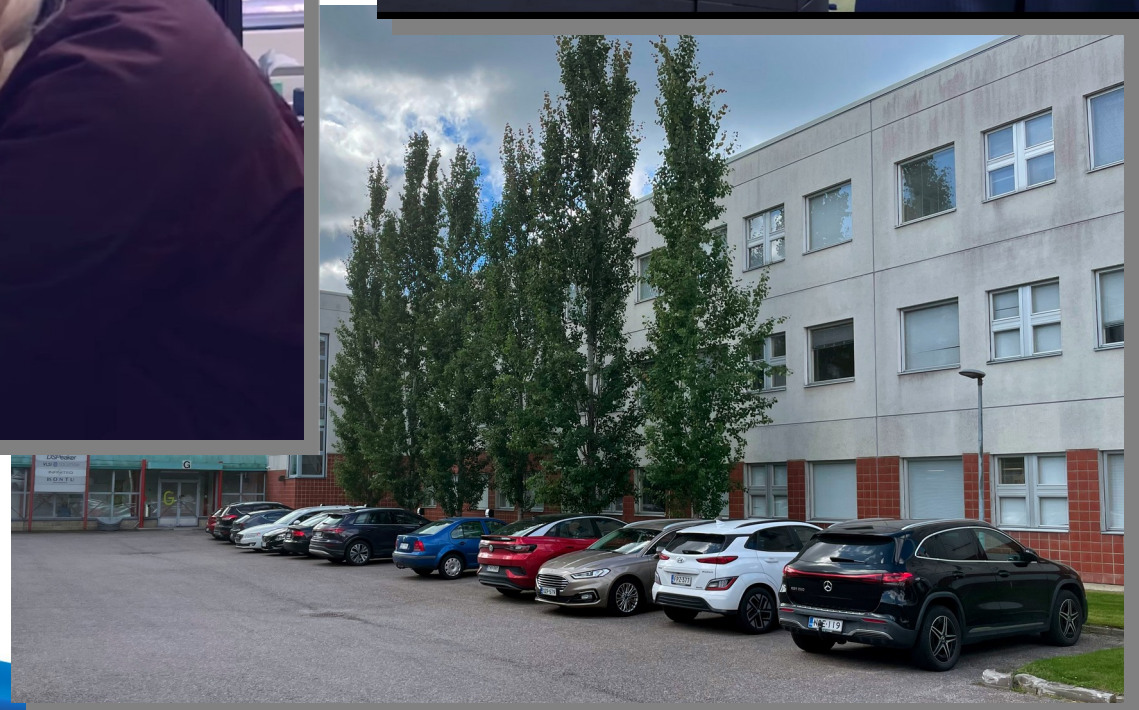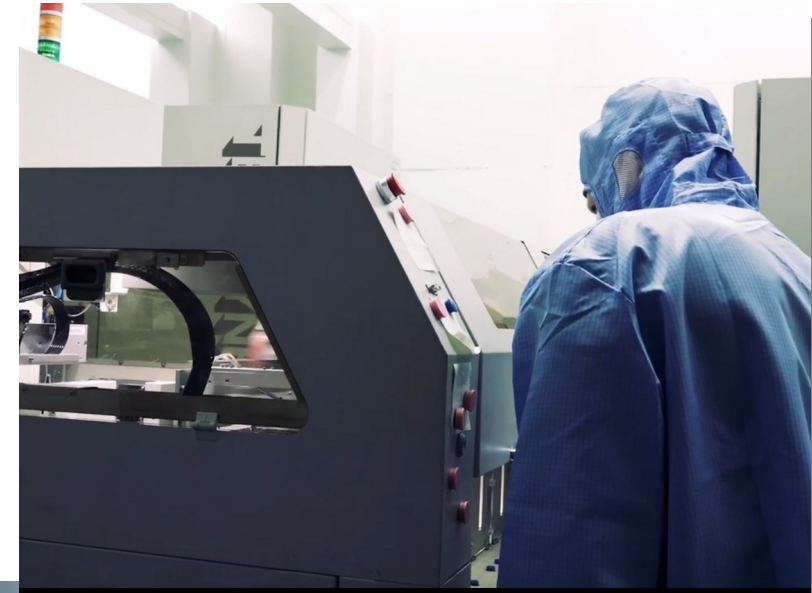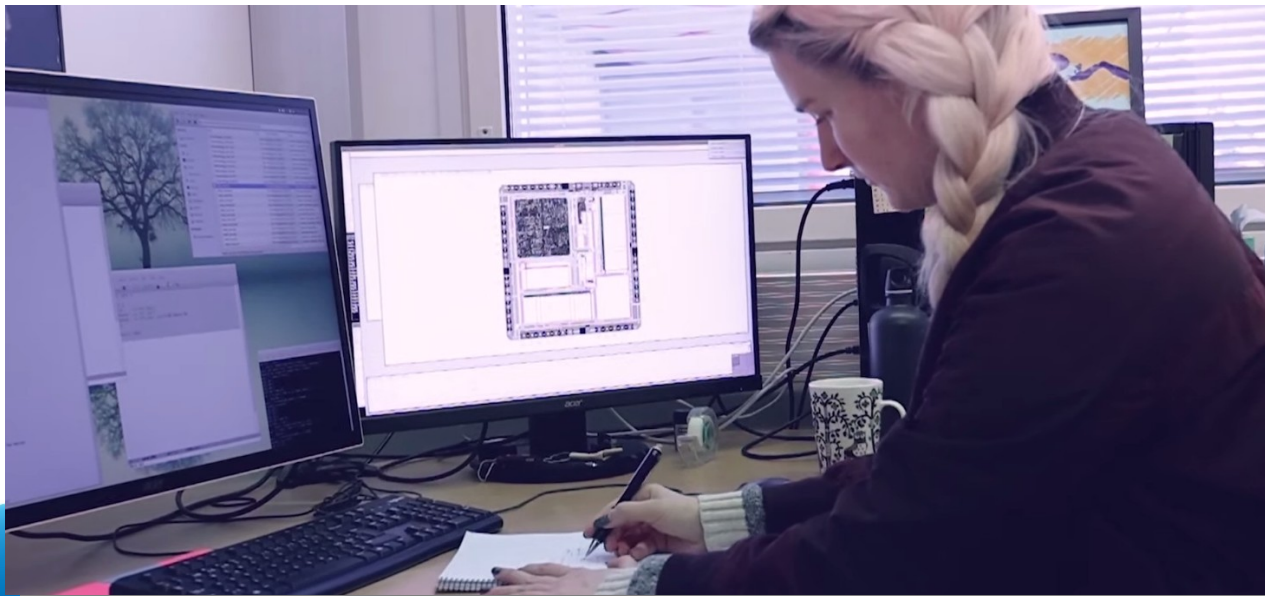# Fabless Model of VLSI Solution

Teppo Karema

28 August 2025

VLSI Solution

- Office 1000m² at Hermia, Tampere
- Clean room 250m²
- SMT protoline & warehouse 300m²

What we are

- Fabless except testing

- Product company (VS…)
    - Audio, IoT, and Industrial markets
    - Sales through distributors

- Service company
    - Design and production services
    - IP licensing
    - Direct sales

- Totally about 80M ICs manufactured
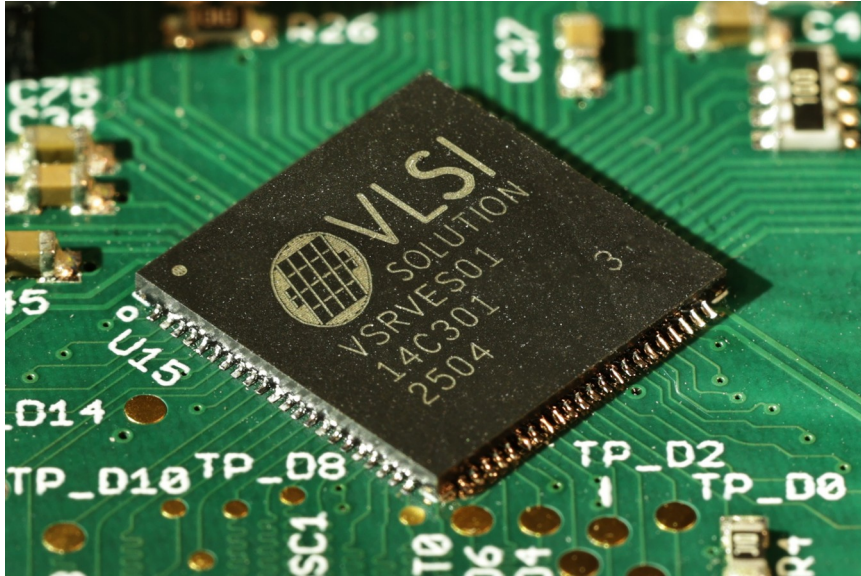
- Core competence is IC design

Latest achievement: VSRVES01

Tamperelainen VLSI Solution yhdisti Linuxin ja RISC-V:n audioprosessorissa

Julkaistu: 30.05.2025

Features of VSRVES01

- All IP designed by VLSI
- Combo of two our processors:
  - 32-bit RISC-V Linux core (VSRV1)
  - 16/32-bit DSP core (VSDSP6)
- LPDDR2 Memory interface
- Ethernet, USB, etc peripherals
- Analog line-in and line-out
- DEMO PCB: Audio streaming over ethernet, web server, telnet, etc.

Co-funded by the European Union

BUSINESS FINLAND

TRISTAN RISC-V

SoC HUB

Foundly Model Variants

IDM*	DESIGN	WAFER PROCESS	ASSEMBLY & TEST	SHIP
Fab-lite	DESIGN	WAFER PROCESS	ASSEMBLY & TEST	SHIP
Fabless	DESIGN	WAFER PROCESS	ASSEMBLY & TEST	SHIP
Non-semi	DESIGN	WAFER PROCESS	ASSEMBLY & TEST	SHIP

VLSI SOLUTION
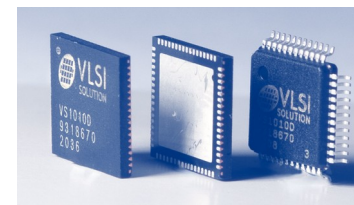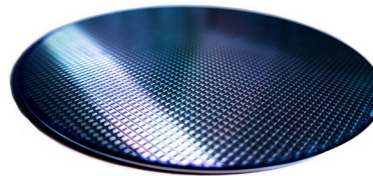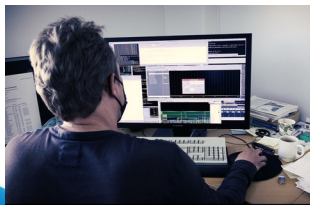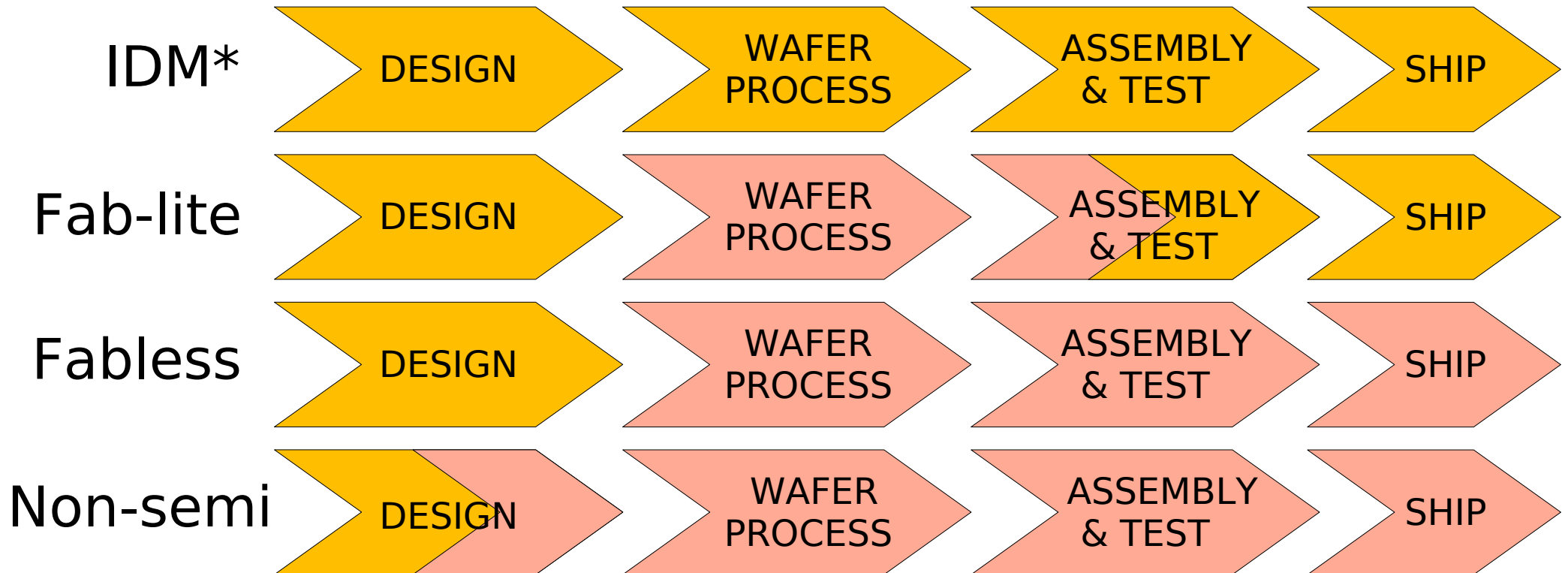
*IDM=Integrated Device Manufacturer

Overview of VLSI's Fab-lite model

DONE BY VLSI

OUTSOURCED

R&D project

Samples (untested)

Design → MPW Wafer Fabrication → Blind Assembly → Evaluation, Characterization, Pre-qualification → Samples (tested)

Typically 2-3 rounds

Transfer to production

Qualification

Production masks → Wafer Fabrication → Blind Assembly → Final Test → QA & Dry Pack → Product

Production

Untested inventory

Prod. Planing → Wafer Fabrication → Wafer Test (opt) → Assembly → Final Test → QA & Dry Pack

Wafer inventory

Product inventory

Details of R&D project

In-house IP

External IP

Application SW

Package Design

Pre-competive R&D

SW+HW Co-Design & Verification

Masks

tapeout

MPW Wafer Fabrication

Blind Assembly

Lab. Testing

samples

Char. Testing

Samples Testing

Pre Qual.

CLEAN-ROOM

Appl. Test

VLSI's EDA tools

Licensed EDA tools

LAB equipment

DONE BY VLSI   OWNED BY VLSI

OUTSOURCED

DONE BY CUSTOMER

VLSI SOLUTION

Details of Production

DONE BY VLSI
OUTSOURCED
OWNED BY VLSI

Consumables Inventory

Leadframes, Substrates

Sockets, Suction cups

Prod. Planing → Wafer Fabrication → Wafer Test (optional) → Assembly → Final Test → QA & Dry Pack → Inventory → Ship to customers

Probecard

Loadboard

Lead/ball scan, QA, Bake

Manufacturing Equipment:
2 testers, 7 handlers, 1 prober, 3 inspection machines, 2 dry pack lines, 7 dry cabinets, etc.

VLSI SOLUTION
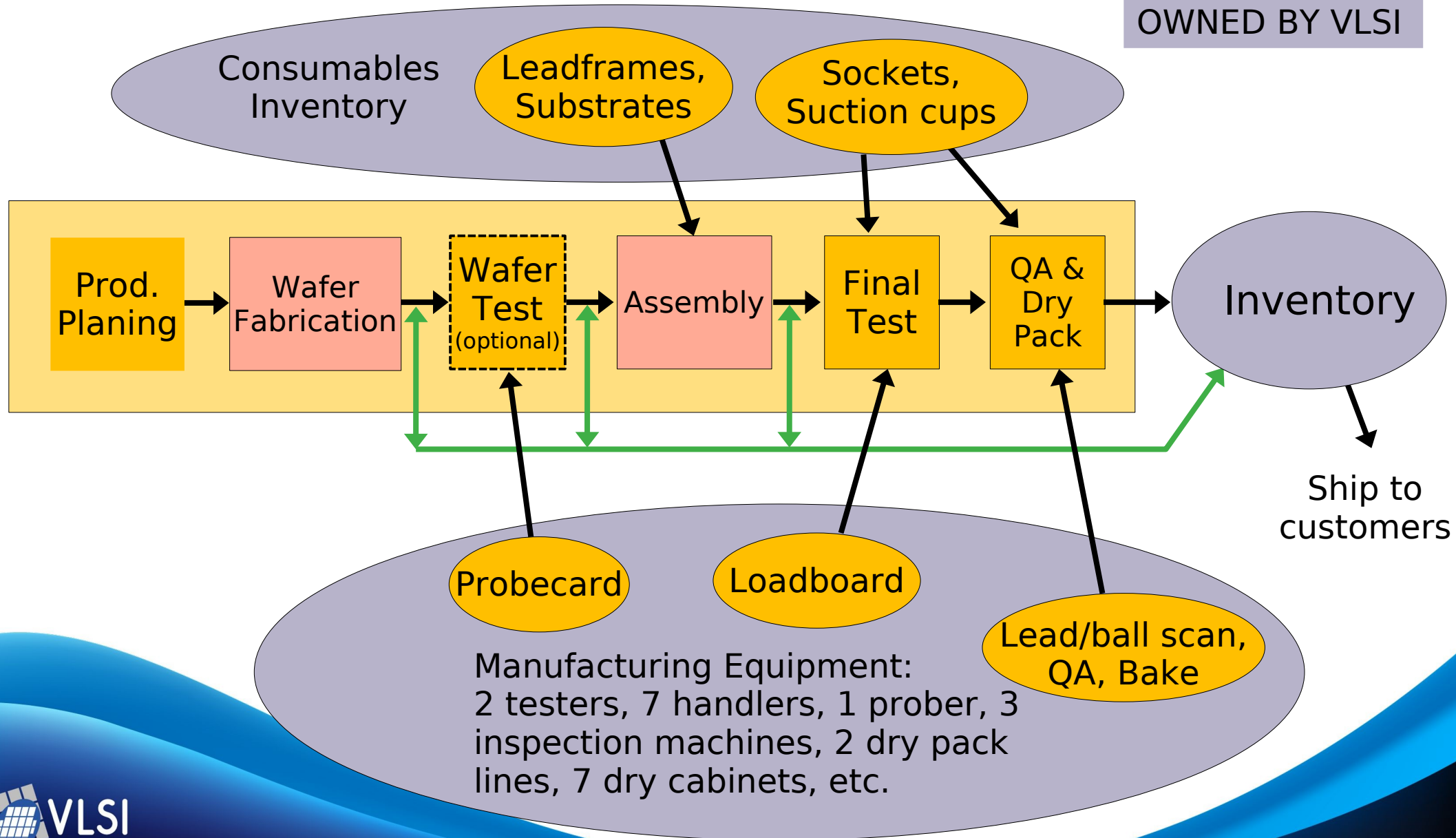
Highlights of VLSI's Foundry Model

Fab-lite manufacturing

- Allows "full" control of the manufacturing
- Has moderately low capital requirement
- Needs only a few people
- Easy to scale up

In-house testing

- DFT becomes included in the design flow
- Reduces Lead times and inventories
- Fast handling of quality issues

VLSI SOLUTION